Amendments to the Specification:

Please replace the paragraph beginning at page 5, line 1 with the following amended paragraph:

Functional microengines ~~microengines~~ 22a-22f each maintain a plurality of program counters...

Please replace the paragraph beginning at page 12, line 18 with the following amended paragraph:

The processor core 20 includes a RISC core 50 implemented in a five stage pipeline performing a ~~single cycle~~ shift of one operand or two operands in a single cycle, provides multiplication support and ...

Please replace the paragraph beginning at page 24, line 19 with the following amended paragraph:

The coding rules of these two paradigms could be significantly different with regard to issuing memory references and context switching. In the real time case, the goal is to issue as many memory references as soon as possible in order to minimize the memory latency incurred by those references. Having issued as many references as early as possible the goad would be to rerform as many computations as possible in the microengines ~~as possible~~ in parallel with the references. A computation flow that corresponds to real-time operation is: